

DUAL GATE LAYOUT FOR THIN FILM TRANSISTOR

FIELD OF THE INVENTION

5 [0001] The present invention relates to a dual gate structure of thin film transistor for liquid crystal display (LCD), and more particularly to a dual gate with at least one gate channel along data line for low temperature polysilicon LTPS LCDs so as to inhibit leakage current and provide picture resolution improvement.

BACKGROUND OF THE INVENTION

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[0002] A liquid crystal display (LCD) is a flat display with properties of low power consumption, low significantly, space occupation and weight in comparison with a conventional cathode ray tube (CRT) and without curve surface as a CRT display has. Hence, the liquid crystal display has widely been applied in all sorts of
15 merchandises, including consumptive electronic products, such as pocket calculators, electronic dictionaries, watches, mobile phones, portable notebooks, communication terminals, display panels, desk-top personal computers, and even high dpi (dots per inch) television (HDTV) and so on. The most popular display is an active-type thin film transistor liquid crystal displays (TFT-LCD) due to the fact
20 that the viewing angle, response time and the contrast performance are much better than that passive type LCD.

[0003] For a long term, amorphous silicon is a main material for TFT manufacture in TFT-LCD device. However, nowadays, another choice is provided, forming transistor using polysilicon is found superior to amorphous silicon. The
25 low temperature polysilicon type TFT-LCD (LPTFT-LCD) may even become a main stream due to the better performance of carrier mobility in polysilicon than in

amorphous. Another advantage of LPTFT-LCD had is the driving circuit can be formed simultaneously with the pixel TFT fabrication. Therefore, LPTFT-LCD can provide a faster switched speed than other types LCD.

[0004] Certainly, LTPS TFT-LCD has some drawbacks need to be overcome. For instance, the device usually has a rather large leakage current during TFTs turn off. To overcome this defect, Inoue et al. proposed a concept of dual gate TFT structure to inhibit the problem of leakage current, as described in the U.S. patent No. 5,693,959. Another method is provided by Ha et al. in the U.S. patent No. 5,940,151; the patent provides lightly doped drain (LDD) technique to alleviate the leakage current problem.

[0005] The present invention concentrates to the dual gate structure of TFTs. FIG. 1A is a top view of the dual gate structure of TFTs, and FIG. 1B is a cross-sectional view along cut-line a-a' of FIG. 1 A. The numeral 909 is denoted a polysilicon layer, which is formed to constitute a heavily doped source region 909a, a lightly doped source region 909b, a first channel 909c, a lightly doped region 909d, which is in between dual gate, a second channel 909d, a second channel 909e, a lightly doped drain region 909f, and a heavily doped drain region 909g. The scan line 903 includes dual gates, one over the first channel 909c and the other over the second channel 909e. The signal line 904 usually made of aluminum is contacted to the heavily doped source region 909a through source contact 910. The drain metal line is connected to a transparent conductive electrode by means of through-hole 913 and drain contact 911 to the heavily doped drain region 909g.

[0006] The forgoing dual gate provided two gates in parallel and formed along the scan line. Unfortunately, in the design of color filter layout, the primary colors: red, blue, and green are usually along scan line. As a result, the resolution of display will suffer some limits. Since, the total lengths of two channel 909c,

909e and the interval in between 909d will be restricted owe to the constraints of lithographic machine for TFT. Since the problem of the pixel is crowded along scan line direction. However, there is no such problem along the data line. Three sub-pixels for three primary colors are not along this direction. By contrast, it provides more process windows. Subsequently, an object of the present invention is to provide a method, which is to reshuffle the positions of the dual gate. Some or part of the loadings of dual gate on the scanning line is shared by the signal line and thus solve the forgoing problem.

10 SUMMARY OF THE INVENTION

[0007] The primary object of the present invention is to provide a TFT with a dual gate structure for a low temperature polysilicon LCD to inhibit current leakage.

[0008] The second object of the present invention is to improve the issue of about conventional dual gate structure, which both of the gates are along scanning line that inferior to the high resolution.

[0009] Five preferred embodiment are disclosed. In the first preferred embodiment, a polycrystalline silicon having a stair shaped in geometry from top view formed on a substrate for a source region, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region formation. The polycrystalline silicon layer having a vertical section and a horizontal section intersect, respectively, with a scanning line, and an I-shaped extension portion thereof to form a first gate channel and a second gate channel.

[0010] In the second preferred embodiment, the polycrystalline silicon having a L-shaped in geometry from top view formed on a substrate for a source region at an end of horizontal section, a first doped region, a first gate channel, a second

doped region, a second gate channel, a third doped region, and a drain region at an end of vertical section formation. The polycrystalline silicon layer having a vertical portion intersects with a scanning line, and a horizontal portion of L-shaped extension portion to form a first gate channel and a second gate channel.

5 [0011] In the third preferred embodiment, the polycrystalline silicon having a L-shaped in geometry from top view formed on a substrate for a source region at an end of horizontal section, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region at an end of vertical section formation. The polycrystalline silicon layer having a
10 horizontal section and a vertical section intersect, respectively, with an I-shaped extension portion and scanning line to form a first gate channel and a second gate channel.

[0012] In the fourth preferred embodiment, the polycrystalline silicon having a L-shaped in geometry from top view formed on a substrate for a source region at
15 an end of horizontal section, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region at an end of vertical section formation. The polycrystalline silicon whose vertical section intersects with a scanning line and a horizontal portion of L-mirror shaped extension portion to form a first gate channel and a second gate channel.

20 [0013] In the fifth preferred embodiment, the polycrystalline silicon having a L-shaped in geometry from top view formed on a substrate for a source region at an end of horizontal section, a first doped region, a first gate channel, a second doped region, a second gate channel, a third doped region, and a drain region at an end of vertical section formation. The polycrystalline silicon layer having a
25 horizontal section and a vertical section intersect, respectively, with a vertical section and a horizontal section of a LI-shaped extension portion to form a first

gate channel and a second gate channel.

BRIEF DESCRIPTION OF THE DRAWINGS

5 [0014] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0015] FIG. 1A is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the present invention.

10 [0016] FIG. 1B is a cross-sectional view illustrating a dual gate structure of a TFT-LCD in accordance with the prior art.

[0017] FIG. 2A is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the first preferred embodiment of the prior art.

15 [0018] FIG. 2B is a cross-sectional view illustrating a dual gate structure of a TFT-LCD in accordance with the first preferred embodiment of the present invention.

[0019] FIG. 3 is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the second preferred embodiment of the present invention.

20 [0020] FIG. 4 is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the third preferred embodiment of the present invention.

[0021] FIG. 5 is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the fourth preferred embodiment of the present invention.

[0022] FIG. 6 is a plan view illustrating a dual gate structure of a TFT-LCD in accordance with the sixth preferred embodiment of the present invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] In addition to large scales is a generic trend for LCD monitors or LCD television, another trend is to raise the resolutions so as to improve the picture quality. Due to the dark leakage current problem, dual gate is a common
5 approaching to solve the leakage current of LTPS TFT-LCDs. However, conventional dual gate structure is detrimental to the resolution improvement because the dual gates are common formed along the scanning line. The structure of the present invention disclosed can resolve such problem.

[0024] The following description is presented to enable one of ordinary skill
10 in the art to make and use the invention and is provided in the context of a patent application and its requirement. Various modifications to the preferred embodiment and generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the
15 principles and features described herein. For example, the present invention will be described in the context of using n-type conductive impurities which is just for illustrating convenience, one of ordinary skill in the art will readily recognize that p-type impurities could be here. And its use would be within the spirit and scope of the present invention.

20 [0025] The present invention proposed several embodiments and will be described as follows:

[0026] According to the first preferred embodiment, referring to FIG. 2A, a top view for one pixel layout. The polycrystalline silicon layer 100 formed on the glass substrate presents as a stair-shaped having regions including 100A,
25 100B, 100C, 100D, 100E, 100F, 100G, 100H, and 100I. The stair-shaped polycrystalline silicon layer 100 intersects with the scanning line 120 and its I-

shaped extension portion by two regions. One is formed as the first channel 100C, and the other is the second channel 100G. Two regions 100B, 100D abutting both sides of the first channel 100C are n-type lightly doped regions. Side regions 100F, 100H abutting the second channel 100G are n-type lightly doped regions 100F 100H too. To further reduce the resistance between channel regions 100C and 100G, one n+ heavily doped region 100E is usually included. Still, the n+ heavily doped source region 100A is contacted with the data line 130 through contact windows 132. The data line 130 is made of metal such as aluminum. The n+ heavily doped drain region 100I is contacted with the storage capacitor (not shown) and connected to the first interconnect line 150, which is formed on the first inter-level dielectric layer 180 through contact windows 133 and further through a via 162 to connect the transparent conductive electrode 160, which is formed on the second inter-level dielectric layer 190.

[0027] The geometry of regions 100D, 100E, and 100F presented as right angle distributed, as is shown in the figure. It is not intended to limit the claim scope. It can be other geometry, for example they can be presented as arc-shaped or a shortest line between the channels 100 C and 100G.

[0028] The second preferred embodiment is shown in FIG. 3, which is a top view. The polycrystalline silicon layer 200 formed on the glass substrate presents as a L-shaped having regions including 200A, 200B, 200C, 200D, 200E, 200F, and 200G. The L-shaped polycrystalline silicon layer 200 intersects with the scanning line 220 and its L-shaped extension portion by two regions. One is formed as the first channel 200C, and the other is the second channel 200E. As aforementioned in the first preferred embodiment, an insulating layer is formed before forming gate metal layer 220. the regions abutting both sides of the first channel 200C and the second channel 200E are n-type lightly doped regions 200B, 200D and 200D, 200F,

respectively. Still, the n+ heavily doped source region 200A is contacted with the metal data line 230 through contact windows 232. The n+ heavily doped drain region 200G is contacted with the storage capacitor (not shown), the first interconnect line (not shown) and the transparent conductive electrode 260. The detailed descriptions are as first preferred embodiment.

[0029] Worthwhile if the channel 200C does not distant from the channel 200E, one n-lightly doped region 200D formed is enough. However, the n-lightly doped region 200D can also have a heavily doped region 200D' in it to reduce resistance.

[0030] The third preferred embodiment is shown in FIG. 4, which is a top view. The polycrystalline silicon layer 300 formed on the glass substrate presents as a L-shaped having regions including 300A, 300B, 300C, 300D, 300E, 300F, 300G, 300H, and 300I. The L-shaped polycrystalline silicon layer 300 intersect with the scanning line 320 and its I-shaped extension portion by two regions. One is formed as the first channel 300C, and the other is the second channel 300G. As described in the first preferred embodiment, an insulating layer is formed before forming gate metal layer 320. the regions abutting both sides of the first channel 300C and the second channel 300G are n-type lightly doped regions 300B, 300D and 300F, 300H, respectively. Still, the n+ heavily doped source region 300A is contacted with the metal data line 330 through contact windows 332. The n+ heavily doped drain region 300I is contacted with the storage capacitor (not shown), the first interconnect line (not shown) and the transparent conductive electrode 360.

[0031] Similarly, the geometry of regions 300D, 300E, and 300F presented as right angle distributed is not necessary. It can be other geometry, for example they can be presented as arc-shaped or a shortest line between the channels 300 C and 300G. Furthermore, if the channel 300c does not distant from the channel 300G,

for example, less than 1 μm , 1 n-lightly doped region 300D formed is enough. Otherwise, it should have an extra heavily doped region to reduce resistance.

[0032] The fourth preferred embodiment is shown in FIG. 5, which is a top view. The polycrystalline silicon layer 400 formed on the glass substrate presents as a L-shaped having regions including 400A, 400B, 400C, 400D, 400E, 400F, and 400G. The L-shaped polycrystalline silicon layer 400 intersects with the scanning line 420 and its L-mirror-shaped extension portion 421 by two regions. One is formed as the first channel 400C and the other is the second channel 400E. Basically, the fourth preferred embodiment is similar to the second preferred embodiment except, the extension portion of the scanning line is L-mirror-shaped in geometry. Thus, we will not recite them in detail.

[0033] The fifth preferred embodiment is shown in FIG. 6, which is a top view for a pixel. The polycrystalline silicon layer 500 formed on the glass substrate presents as a L-shaped having regions including 500A, 500B, 500C, 500D, 500E, 500F, 500G, 500H, and 500I. The L-shaped polycrystalline silicon layer 500 intersect with the scanning line 520 and its L-shaped extension portion 521 by two regions. One is formed as the first channel 500C, the other is the second channel 500G. The regions abutting both sides of the first channel 500C and the second channel 500G are n-type lightly doped regions 500B, 500D, and 500F, 500H, respectively. Still, the n+ heavily doped source region 500A is contacted with the metal data line 530 through contact windows 532. The n+ heavily doped drain region 500I is contacted with the storage capacitor (not shown), the first interconnect line (not shown) and the transparent conductive electrode 560, as aforesaid in the first preferred embodiment.

[0034] The benefit of the present invention provided is:

[0035] The dual gate structure of the TFT according to the present invention

at least one gate channel is along data line direction. As a result, more pixels can be set along the scanning line and thus the picture resolution can be elevated.

5 [0036] As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure